REMARKS

In the Office Action mailed June 11, 2007, the Examiner noted that claims 2-5, 7, 8, 10-13, 15-18, and 20-22 were pending and rejected claims 2-5, 7, 8, 10-13, 15-18, and 20-22. Claims 17, 21 22 have been amended, no claims have been canceled, new claim 23 has been added; and, thus, in view of the foregoing claims 2-5, 7, 8, 10-13, 15-18, and 20-23 remain pending for reconsideration which is requested. No new matter is believed to have been added. The Examiner's rejections and objections are respectfully traversed below.

OBJECTIONS

The Office Action, on page 2, objected to the specification because the title of the invention was not descriptive. The title of the invention has been amended to recite "COMPUTER AND CONTROL METHOD OF THE COMPUTER FOR PROCESSING AN INTERRUPT" It is respectfully submitted that the title of the invention is descriptive and, therefore, overcomes the objection.

Accordingly, Applicants respectfully request that the objection be withdrawn.

REJECTIONS under 35 U.S.C. § 112

The Office Action, on page 3, rejected claims 2-5, 7, 8, 10-13, 15-18 and 20-22 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The Office Action at page 3 asserted that the specification does not provide support for the recitation of claim 21 of processing plural instructions in parallel. The Office Action further contends that the specification only shows that a plurality of data holding parts may be in parallel, and does not go into any detail on how the operation of these data parts effects the parallel processing of the instructions. The Office Action's rejection is respectfully traversed with an argument.

The Applicants respectfully asserts that the specification contains a written description of the invention and of the manner and process of making and using the invention in full, clear, concise, and exact terms as to enable any person skilled in the art to make and use the same.

The recitation of "processing plural instructions in parallel" is supported by Figure 5 (including instruction execution parts 25, 27, 29, 33, 35 and 37 in parallel) and page 28, lines 8-12 of the Specification, which describes an instruction next to an instruction which has a possibility of being interrupted can be issued without waiting for completion of execution of the instructions which has a possibility of being interrupted. Page 28 of the Specification further states that the computer includes the EPCR 73, the ESR 75, the EAR 77 and the EDR 79 each of which includes a plurality of registers in parallel, where necessary data for returning to original

process from interrupt processing operation is held in these registers in parallel when interrupt occurs. Therefore, an instruction next to an instruction which has a possibility of being interrupted can be issued without waiting for completion of execution of the instruction which has a possibility of being interrupted. As a result, effective rate of operation of hardware can be further improved. Thus, the recitation of "a data holding part holding data on all of instructions being executed at a time when said interrupt starts to occur" is supported by Fig. 5 and Fig. 7 (e.g. holding data on all of instructions being executed).

In view of the foregoing, a person of ordinary skill in the art would be enabled to make and use the recitation of claim 21, for example, of processing plural instructions in parallel in view of the Specification.

Therefore, it is respectfully submitted that claims 2-5, 7, 8, 10-13, 15-18 and 20-22 satisfy the requirements of 35 U.S.C. § 112, first paragraph.

The Office Action, on page 4, rejected claims 2-5, 7, 8, 10-13, 15-18 and 20-22 under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, the Office Action asserted that the idea of storing a plurality of addresses of instructions operating in parallel is unclear because there is no support for the idea in the Specification.

The arguments presented above with respect to the response to the rejection under § 101 is applicable here where appropriate. Specifically, a person of ordinary skill in the art would be enabled to make and use the recitation of claim 21, for example, of processing plural instructions in parallel in view of the Specification. Therefore, it is respectfully submitted that claims 2-5, 7, 8, 10-13, 15-18 and 20-22 satisfy the requirements of 35 U.S.C. § 112, second paragraph.

Accordingly, Applicants respectfully requests that the objection be withdrawn.

REJECTIONS under 35 U.S.C. § 103

The Office Action, on page 4, rejected claims 2, 5, 8, 10, 13, 16-18 and 20-22 under 35 U.S.C. § 103(a) as being unpatentable over Computer Organization & Design (Computer Organziation & Design; Patterson et al.) (hereinafter Patterson) in view of U.S. Patent No. 5,182,811 (Sakamura).

The Office Action, on page 5, asserted that paragraph 1 on page 223 of Patterson teaches "a data holding part holding said instruction when the instruction processing starts." Further, the Office Action acknowledges that Patterson does not teach that there are plural

instructions in parallel and having the memory store the addresses of the plural instructions during the interrupt and relies upon Sakamura to teach this features.

However, claim 21 has been amended to recite:

> A computer which processes plural instructions in parallel, and which performs an interrupt process when an interrupt occurs while an instruction in a program is executed, said computer comprising:
> a data holding part holding data on all of instructions being executed at a time when said interrupt starts to occur,
> wherein the computer performs interrupt processing by an interrupt processing program by reading the data from holding part to return from the interrupt.

By at least the aforementioned features of amended claim 21, by holding data, in the data holding part, on all of the instructions being executed, execution consistency is adjusted by the software. Therefore, the interrupt processing can be performed without decreasing the rate of operation of the hardware.

It is respectfully submitted that neither Patterson nor Sakamura teaches or suggests the aforementioned feature of claim 21.

Specifically, nothing was found in Patterson that describes "data holding part **holding data on all of instructions** being executed at a time when said interrupt starts to occur". Rather, paragraph 1 on page 223 of Patterson describes:

> MIPS detects overflow with an exception, also called an interrupt on many computers. An exception or interrupt is essentially an unscheduled procedure call. The address of the instruction that overflowed is saved in a register, and the computer jumps to a predefined class to invoke the appropriate routine for that exception. The **interrupted address is saved** so that in some situations the program can continue after corrected code is executed.

Stated another way, Patterson describes **storing an address** of an instruction **that caused the exception**. Therefore**, storing an address** of an instruction that caused an exception does not constitute **holding data on all instructions** being executed when the interrupt starts.

With respect to Sakamura, nothing was found in Sakamura that describes the aforementioned features of claim 21. Rather, Sakamura is related to an exception, interrupt and trap handling apparatus which fetches addressing and context data using a single instruction following an interrupt (see Sakamura, Abstract). Specifically, Sakamura describes a device for **storing** 2024 **in an external memory** 2020 **the first information group** to be an internal state that is the initial state of the selected EIT process (see Sakamura, col 2, lines 13-37). Sakamura further describes storing in the generated address of the external memory a second information group to be a candidate. However, **storing the first information group** as described in

Sakamura does not constitute "holding data on all instructions being executed at a time when said interrupts starts to occur".

Further, nothing was found in Patterson and/or Sakamura that describes the feature of "performing interrupt processing by an interrupt processing program by reading the data (e.g. on all of instructions being executed) from the data holding part" as recited in amended claim 21.

Therefore, it is respectfully submitted that the entire combination of Patterson and Sakamura is deficient. Thus, it is respectfully submitted that independent claim 21 patentably distinguishes over the combination of Patterson and Sakamura. Claims 17 and 22 have been amended similarly to that of claim 21. Therefore, it is respectfully submitted that claims 17 and 22 patentably distinguish over the combination of Patterson and Sakamura for reasons similar to those mentioned above with respect to claim 17. The dependent claims patentably distinguish over the combination of Patterson and Sakamura for the same reasons as their respective base claims.

The Office Action, on page 5, rejected 3, 4, 7, 11, 12 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Patterson in view of Sakamura and further in view of U.S. Patent No. 6,098,167 (Cheong).

It is respectfully submitted that dependent claims 3, 4, 7, 11, 12 and 15 patentably distinguish over the combination of Patterson and Sakamura for the same reasons as their respective base claims. Further, nothing was cited in Cheong that cures the deficiencies of Patterson and Sakamura. Therefore, it is respectfully submitted that dependent claims 3, 4, 7, 11, 12 and 15 patentably distinguish over the combination of Patterson, Sakamura and Cheong.

Accordingly, Applicants respectfully request the rejections be withdrawn.

NEW CLAIM

New claim 23 has been added to emphasize the feature of performing interrupt processing using the interrupt processing instructions stored in the data holding unit to return from the interrupt. It is respectfully submitted that nothing was found in the combination of references that teaches or suggests the aforementioned features of new claim 23. Therefore, it is respectfully submitted that claim 23 patentably distinguishes over the combination of references.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. Further, all pending

claims patentably distinguish over the prior art. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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